

## A 90nm CMOS Integrated Nano-Photonics Technology for 25Gbps WDM Optical Communications Applications

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**Abstract:** The first sub-100nm technology that allows the monolithic integration of optical modulators and germanium photodetectors as features into a current 90nm base high-performance logic technology node is demonstrated. The resulting 90nm CMOS-integrated Nano-Photonics technology node is optimized for analog functionality to yield power-efficient single-die multichannel wavelength-multimultiplexed 25Gbps transceivers.

**Introduction:** Novel optical communications standards addressing emerging large volume applications in datacenters, supercomputers, and server backplanes require cost-effective and power efficient 25Gbps optical transceivers [1]. Integration of analog and mixed-signal circuits (AMS) together with optical components such as modulators, photodetectors (PD), and wavelength division multiplexing (WDM) filters is considered a viable approach for significantly decreasing the cost of optical transceivers and for their massive deployment in large scale systems [2,3].

**Technology Features:** Single-die 25Gbps multichannel integrated WDM transceivers require technology optimization for yielding fast, low-power AMS circuits rather than optimization for digital performance, due to relatively small amount of digital circuitry needed for target applications. The choice of the base foundry 90nm bulk technology with gate length of 63nm [4] is dictated by the relatively high initial  $F_t > 150\text{GHz}$  for high speed NMOS devices (HS NMOS) [5], high trans-conductance, low variability, and the ability to control short channel effects down to 35nm gate length [6].

To yield deeply scaled nanophotonics features, a high-resistivity SOI substrate with  $2\mu\text{m}$  BOX is utilized as a base for 90nm CMOS-Integrated Nano-Photonics (CINP) technology (see Fig.1 and Fig.2). The gate length was scaled below 50nm to increase the  $F_t$  in order to achieve stable 25Gbps performance. The base 90nm technology flow was optimized to yield HS NFET devices with high  $G_m$  gain ( $1\text{mS}/\mu\text{m}$  at  $V_{dd}=1\text{V}$ ), large  $I_{dsat}$  ( $0.9\text{mA}/\mu\text{m}$  at  $V_{dd}=1.2\text{V}$ ), and low overlap capacitance ( $C_{ov}=0.29\text{fF}/\mu\text{m}$ ), while keeping digital device characteristics intact. Fig.3 shows representative  $I_{ds}-V_{gs}$  and sub-threshold characteristics for the HS NMOS and HS PMOS devices for the 90nm CINP node. The DC characteristics for both HS and standard devices are summarized in Table 1, showing a good compromise in technology optimization for both AMS and digital performance requirements.

Passive nanophotonics features (see Fig.4 and Fig.5), integrated into the shallow trench isolation at no additional cost, include optical waveguides, waveguide crossings, directional couplers, lateral fiber couplers, temperature-tolerant ( $\pm 30^\circ\text{C}$

drift) WDM filters (Fig.4), and vertical grating couplers (Fig.5). The active nanophotonics features, which require minimal add-on mask levels, include modulators (Fig.1) and Ge PD (Fig.2), performing electrical-to-optical and optical-to-electrical conversion, respectively. The modulator requires a shallow silicon etch and shares doping levels with CMOS modules [2, 3]. The waveguide-integrated Ge PD is integrated into the FEOL flow using a “Ge-first” approach, utilizing deposition prior to source-drain activation anneal [7].

**RF Performance:** Fig.6 shows the  $S_{21}$  measurements of a Ge PD and a modulator. At a bias of  $V_b=-2\text{V}$ , the 3dB bandwidth of the Ge PD exceeds 20GHz, sufficient for 25Gbps performance. The modulator active phase shifter was designed as a horizontal p-n junction to achieve high capacitance  $C_j = 0.63\text{fF}/\mu\text{m}$  and a figure of merit  $V\pi L$  of  $1.2\text{V}\cdot\text{cm}$  at reverse bias  $V_b=-1\text{V}$ . The wafer-to-wafer variability of  $C_j$  is controlled within  $\sigma=1.5\%$  (Fig.7). The  $S_{21}$  curve of such a p-n junction modulator is measured at  $V_b=-0.5\text{V}$  showing 3dB bandwidth exceeding 30GHz.

A library of passive electrical features (inductors, capacitors, resistors) of the base 90nm bulk technology, when fabricated on a high-resistivity SOI substrate, demonstrate significantly improved RF properties. As shown in Fig.8, up to 50% improvement of a compact peaking inductor  $Q$  is evident when fabricated with 90nm CINP technology.

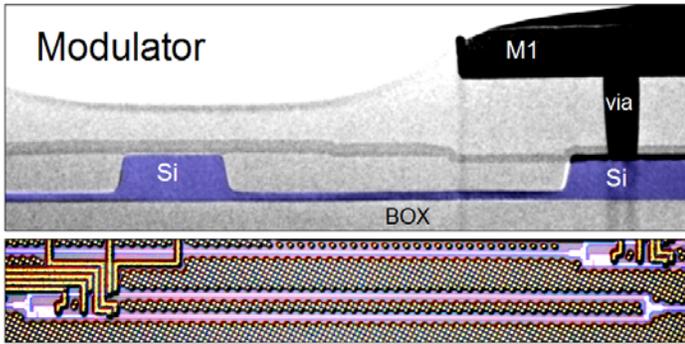
**Transceiver Circuits:** Fig.9 shows measurements of the rise time for a differential CML inductively peaked output buffer fabricated in 90nm CINP technology when compared to the base 90nm bulk technology. Scaling the gate length in CINP technology helps to maintain the rise time below 12 ps even for extended temperature range up to  $90^\circ\text{C}$  consistent with requirements for 25Gbps applications.

Fig.10 shows the performance of a monolithically integrated receiver consisting of a Ge PD, transimpedance amplifier (TIA), six cascades of limiting amplifiers (LA), and an output buffer. The electrical eye diagram of the receiver, measured with  $1.54\mu\text{m}$  light modulated at 25Gbps, shows a good performance.

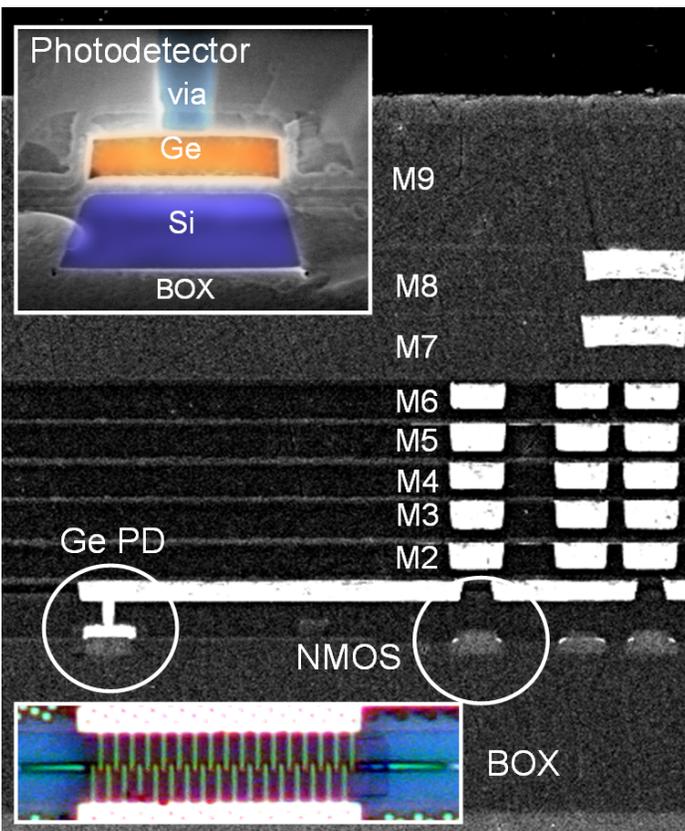
Further improvements in speed, power efficiency and the number of parallel channels is expected with the use of advanced circuit designs leveraging the improved RF characteristics of 90nm CINP optical and electrical features [8].

**Conclusion:** The reported 90nm CINP technology is well positioned for manufacturing cost-effective single-die 25Gbps multi-channel WDM optical transceivers.

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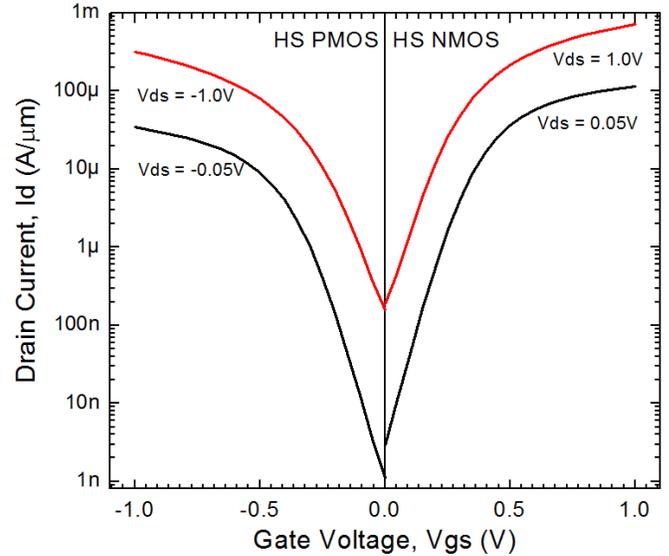
**Figure 1.** Cross-sectional TEM view of a 90nm C1NP metal stack with Si modulator embedded into the front-end. Optical microscope top-down image is shown on the bottom.



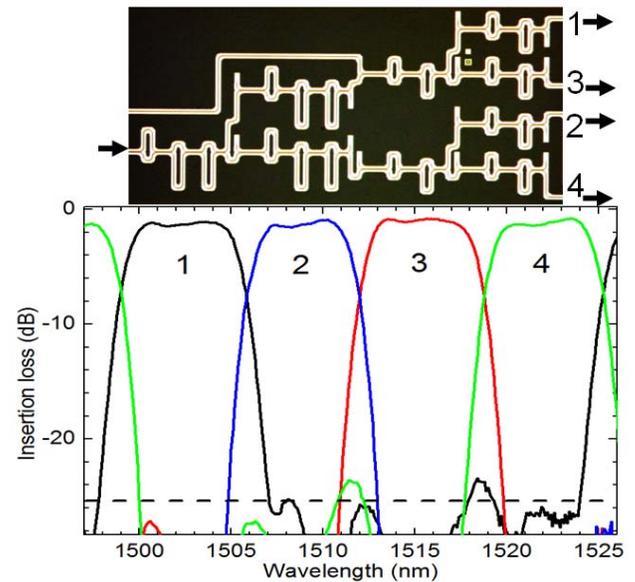
**Figure 2.** Cross-sectional SEM view of a 90nm C1NP metal stack with Ge PD embedded into the front-end. Zoomed-in image of a photodetector is shown on top left. Optical microscope top-down image is shown on the low left.

	Units	HS Nfet	HS Pfet	Std Nfet	Std Pfet
<b>Vt sat</b>	V	0.17	-0.12	0.25	-0.25
<b>Id sat</b>	uA/um	730	310	660	250
<b>SubVt slope</b>	mV/dec	100	100	100	100
<b>Ioff</b>	nA/um	190	170	40	5
<b>Cgd</b>	fF/um	0.29	0.29	0.29	0.29
<b>Gmsat</b>	uS/um	1040	495	1000	470

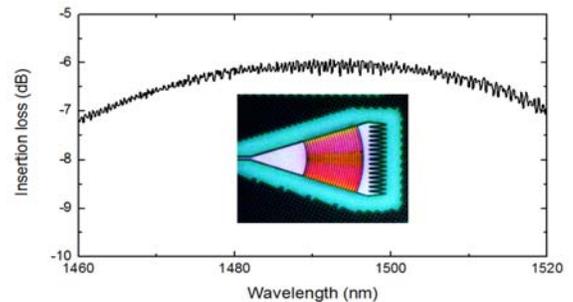
Table 1. 90nm C1NP technology node high-speed (HS) analog and standard (Std) digital devices at Vd=1V



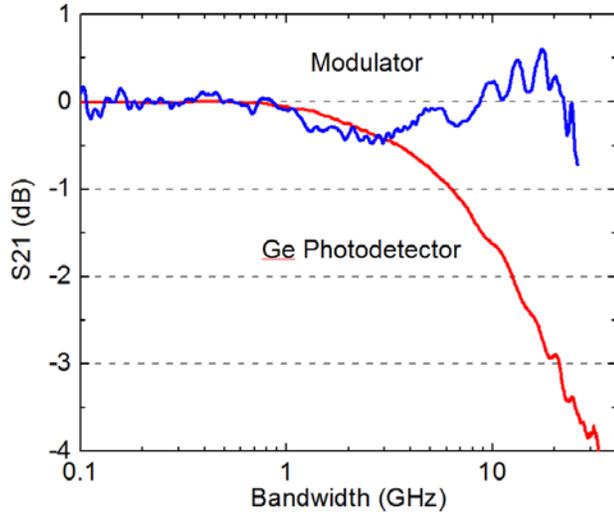
**Figure 3.** Id-Vg characteristics showing sub-threshold behavior for 90nm C1NP HS NMOS and HS PMOS



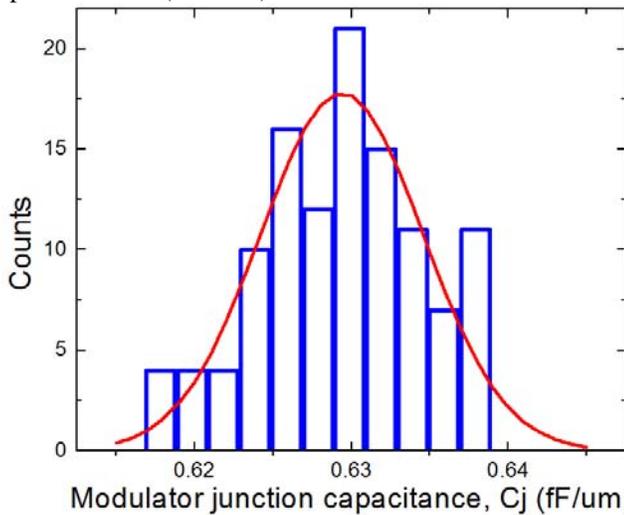
**Figure 4.** Measured insertion loss for a 4 channel WDM filter with 850GHz channel spacing, 500GHz flat-top, 0.3dB in-band ripple, 1.2dB insertion loss and -24dB crosstalk.



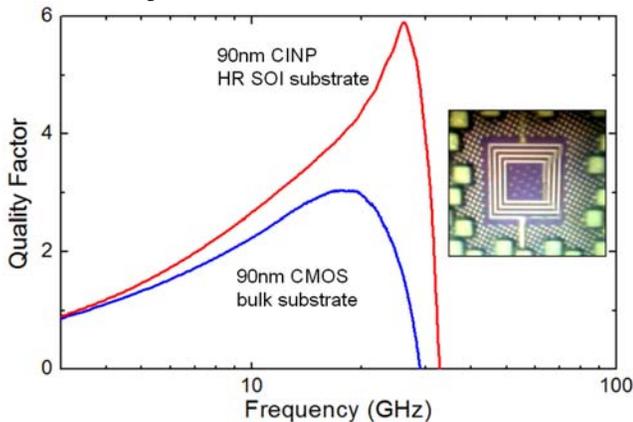
**Figure 5.** Measured insertion loss for a vertical grating coupler for wafer-scale in-line testing of nanophotonics features. Optical microscope top-down image of a device is shown in the inset.



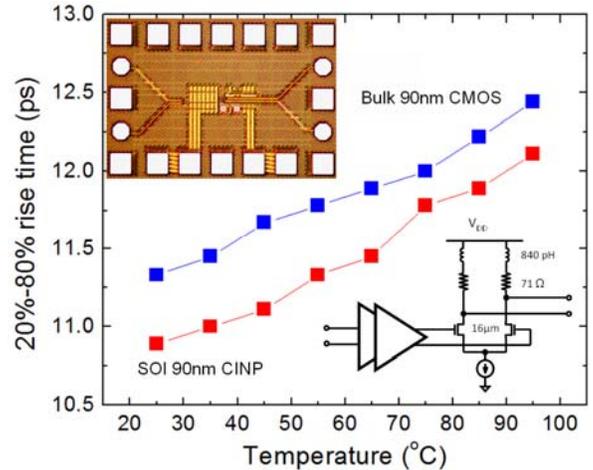
**Figure 6.** Measured S21 response of a modulator ( $V_b=-0.5V$ ) and Ge photodetector ( $V_b=-2V$ ).



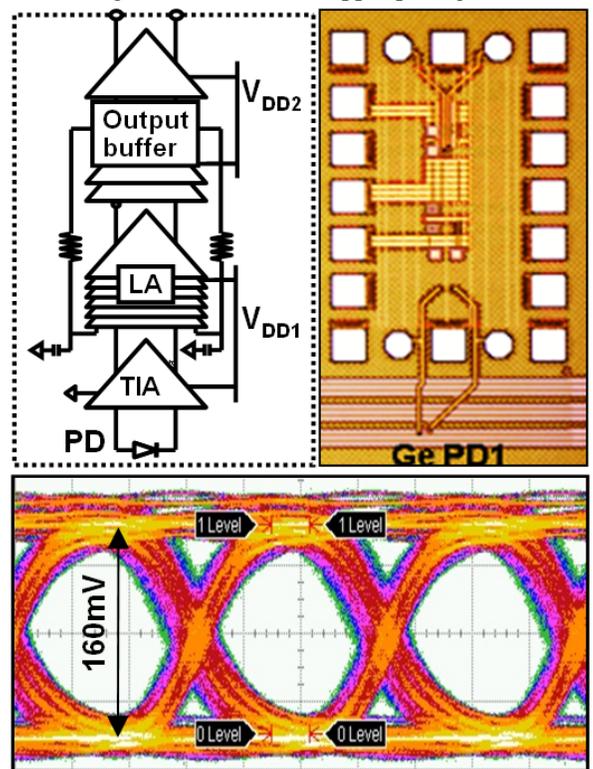
**Figure 7.** Histogram of the wafer-to-wafer variation of modulator pn-junction capacitance  $C_j$  measured across five wafers (115 samples)



**Figure 8.** Measured quality factor of a 1600pH compact peaking inductor fabricated in base 90nm technology on a bulk substrate and in 90nm CIMP technology on high-resistivity SOI substrate.



**Figure 9.** Comparison of measured rise times for an inductively-peaked output LA buffer fabricated using base 90nm bulk and 90nm CIMP technologies driven with 0.5Vpp input signal.



**Figure 10.** 25Gbps performance of integrated Ge receiver fabricated in 90nm CIMP technology. Figure shows schematics (left top), die photograph (right top), and 25Gbps electrical eye diagram

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